"As to claim 14, Graettinger et al., Figure 14, discloses a method for fabricating a semiconductor memory device comprising: forming a pad (1100) on a semiconductor substrate (110); forming an interlayer dielectric layer (400) on the pad and semiconductor substrate for insulating the pad;... "

Applicants disagree with the Examiner's interpretation of Graettinger et al.

First, reference number 400 of Graettinger et al. is not an interlayer dielectric layer (ILD). Further, the ILD is illustrated by reference number 150 of Graettinger et al. Reference number 400 is an insulating spacer.

Second, neither the insulating spacer 400 nor the ILD 150 is formed on the so-called "pad" 1100. Rather, reference number 1100 of Graettinger et al. is a silicide region formed after the insulating spacer 400 and the ILD 150 are formed.

In the Office Action, the Examiner further states:

"As to claim 14, Graettinger et al., Figure 14, discloses a method for fabricating a semiconductor memory device comprising ... forming a bit line stack (120), which includes bit line spacers (Figure 2, element 130), on the interlayer dielectric layer; ... "

Again, Applicants disagree with the Examiner's interpretation of Graettinger et al.

Clearly, the bit line stacks 120 and spacers 130 are formed on the substrate 110 of Graettinger et al., not the ILD 150. As anyone of ordinary skill would attest, the ILD 150 must be deposit after the bit line stacks 120 and spacers 130 are already formed. See FIG. 1 of Graettinger et al.

The Examiner's attention is directed to FIG. 2 of the present application. As recited in claim 14, an interlayer dielectric layer 15 is formed on a pad 13

and a substrate 11 so as to insulate the pad. Then, a bit line stack 23 is formed on the interlayer dielectric layer 15, and bit line spacers 25 are formed at side walls of the stack 23. A storage node contact hole is formed in the interlayer dielectric layer 15 using a self-aligned contact etching so as to expose the pad 13. Finally, as shown in subsequent figures, a contact plug is formed in the contact hole 26.

Graettinger et al. does not teach the aforementioned features of claim 14. That is, referring to FIG. 2 of Graettinger et al., the gate electrodes 120 are formed on an underlying substrate 110, not an interlayer dielectric layer. Further, if even the substrate 110 of Graettinger et al. were somehow considered an interlayer dielectric layer, there is no teaching in Graettinger et al. of self-aligned contact etching of a contact hole in an interlayer dielectric layer that is formed under a gate electrode stack.

For at least the reasons stated above, Applicants respectfully contend that claims 14-20 are not anticipated by Graettinger et al.

Conclusion

No other issue remaining, reconsideration and favorable action upon the claims 14-20 now pending in the application are requested.

Respectfully submitted,

Volentine Francos & Whitt, PLLC

Adam C. Volentine
Reg. No. 33289

One Freedom Square
11951 Freedom Drive, Suite 1260
Reston VA 20190
Tel. (703) 715-0870

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